

ROLL NO. _____

M. Tech. (ECE) – 2nd SEMESTER
ELECTRONIC SYSTEM DESIGN – 13130201
END TERM THEORY EXAMINATION

Time: 03:00 Hours

Maximum Marks – 100

Instructions:

1. Write your Roll No. on the question paper.
2. Candidate should ensure that they have been provided with correct question paper. Complaints in this regard, if any, should be reported to the invigilator on duty in the examination hall within 15 minutes of the commencement of the exams. No complaints shall be entertained thereafter.
3. Attempt any **FIVE** questions. **Q.1** is compulsory. Students are required to attempt **FOUR** questions, selecting **ONE** from each unit. Marks are indicated against each.
4. Draw diagram whenever required.

- Q.1**
- a) Discuss MSI decoder. (04)
 - b) Discuss wired logic. (04)
 - c) Explain AND-OR-Inverter logic. (04)
 - d) What is clock skew. (04)
 - e) Discuss tri-state bus system. (04)

UNIT-I

- Q.2** Discuss the synchronous counter. Design 4-bit Synchronous up/down counter using JK flip flop. (20)
- Q.3** How next state decoder helps in designing & realization of Sequential machines? (20)

UNIT-II

- Q.4** What is the significance of master-slave JK flip flop? Design mater-slave JK flip flop. (20)
- Q.5** Discuss various design steps for traditional synchronous sequential circuits. Take an example to prove your answer. (20)

UNIT-III

- Q.6** Discuss detailed flow diagram for the development of system? (20)
- Q.7** How timing and frequency considerations will affect the system performance? Discuss your answer in Detail. (20)

UNIT-IV

- Q.8** Compare PAL & PLA programmable logic device. Take an example & realize that using both PAL & PLA devices. (20)
- Q.9** Discuss MEV approaches to asynchronous design, in detail. (20)

Roll No. _____

M. Tech.(ECE) - 2nd Semester
Optical Communication – 13130202
END TERM THEORY EXAMINATION

Time: 03 Hours

Max. Marks: 100

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3. Attempt any **FIVE** questions. **Q.1** is compulsory. Students are required to attempt **FOUR** questions selecting **ONE** from each unit. Marks are indicated against each.
4. Draw diagram whenever required.

Q.1 Explain the following-

(4X5=20)

- a) Polarization control
- b) Dispersion shifted and dispersion flattened fibers
- c) Edge Emitting LEDs
- d) Noise in coherent receiver

UNIT-I

- Q.2 Explain block diagram of optical communication system with each component. (20)**
- Q.3 Differentiate between step index and graded index fiber with suitable diagram. How the rays do propagate in graded index fiber? (20)**

UNIT-II

- Q.4 What are fiber losses? Explain its different types. (20)**
- Q.5 List out various advantages of optical fiber communication system over the conventional electrical communication system. (20)**

UNIT-III

- Q.6 Explain the working of P-I-N photodiode. Also explain the factors that limit the speed of response of photodiode. (20)**
- Q.7 What is the population Inversion? Explain the mechanism of Population inversion for three level & four level energy state system. (20)**

UNIT-IV

- Q.8 Explain the working of a heterodyne detection technique suitable for optical fiber communication. (20)**
- Q.9 What are the advantages of a coherent optical communication system? Explain the principle of heterodyne detection used in optical systems. (20)**

Roll No. _____

M. Tech. (ECE) - 2nd Semester
VLSI Design – 13130203
END TERM THEORY EXAMINATION

Time: 03 Hours

Max. Marks: 100

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3. Attempt any **FIVE** questions. **Q.1** is compulsory. Students are required to attempt **FOUR** questions selecting **ONE** from each unit. Marks are indicated against each.
4. Draw diagram whenever required.

Q.1 Attempt all questions:

(4x5=20)

- (a) Differentiate between Depletion and Enhancement type MOSFETs.
- (b) Differentiate between combinational and sequential logic circuits.
- (c) Explain what is meant by a pass transistor.
- (d) Briefly describe a PLA and a FSM.

UNIT-I

- Q.2** Describe the working of a CMOS inverter and draw its stick diagram. **(20)**
- Q.3** Derive the expression of pull-up to pull-down ration of an NMOS inverter which is driven by a network of pass transistors. **(20)**

UNIT-II

- Q.4** Describe the stages involved in a typical NMOS processing cycle. **(20)**
- Q.5** Describe in detail the working of an n-channel depletion type MOSFET. **(20)**

UNIT-III

- Q.6** Describe the need for design rules in VLSI and explain Lambda based rules. Draw the fully labelled circuit diagram and stick diagram of a NAND gate. **(20)**
- Q.7** Describe the concept of propagation delays and explain the working of a CMOS non-inverting superbuffer. **(20)**

UNIT-IV

- Q.8** Describe the concept of scaling on MOS circuits. Differentiate between constant field and Constant voltage scaling. **(20)**
- Q.9** Implement the design of an ALU sub-system. **(20)**

*****ETE MAY/JUNE 2018*****

Roll No. _____

M. Tech(ECE) - 2nd Semester
Wireless Mobile Communication – 13130204
END TERM THEORY EXAMINATION

Time: 03 Hours

Max. Marks: 100

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3. Attempt any **FIVE** questions. **Q.1** is compulsory. Students are required to attempt **FOUR** questions selecting **ONE** from each unit. Marks are indicated against each.
4. Draw diagram whenever required.

- Q.1 Explain the following: (4X5=20)**
- a) What is Paging System?
 - b) Define Time Dispersion.
 - c) How Soft Hand off works?
 - d) Define Signaling & Call Control.

UNIT-I

- Q.2 Explain Channel Assignments Strategies. (20)**
- Q.3 Explain Hand Off Strategies. (20)**

UNIT-II

- Q.4 Explain Okumara model in detail. (20)**
- Q.5 Explain all Diversity Techniques. (20)**

UNIT-III

- Q.6 How FDMA works? Compare FDMA, TDMA & CDMA. (20)**
- Q.7 Explain CSMA in details. (20)**

UNIT-IV

- Q.8 Explain IS-95 in details. (20)**
- Q.9 Explain working of Packet error modeling on fading channels. (20)**

*****ETE MAY/JUNE 2018*****

Roll No: _____

M. Tech. (ECE) - 2nd Semester
Switching System – 13130207
END TERM THEORY EXAMINATION

Time: 03 Hours

Max. Marks: 100

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3. Attempt any **FIVE** questions. **Q.1** is compulsory. Students are required to attempt **FOUR** questions selecting **ONE** from each unit. Marks are indicated against each.
4. Draw diagram whenever required.

- Q.1 Explain the following- (4X5=20)**
- a) Define Erlang and CCS. How are they related?
 - b) Network control processor
 - c) Blocking and stationary probability
 - d) Routing protocol in network management

UNIT-I

- Q.2 (a) What are single stage and multistage switching networks? Compare the strengths and weaknesses of each. (10)**
- (b) What is the need of a hybrid in telephone network? How does it work? (10)**
- Q.3 Write a brief note on switching functions. Explain local and transit traffic switching using suitable diagram. (20)**

UNIT-II

- Q.4 What is centralized SPC? Explain its modes of operation. (20)**
- Q.5 Explain the block diagram of STS switch. Explain various functional entities. (20)**

UNIT-III

- Q.6 What is Markov processes representing traffic. Calculate the blocking probability and stationary probability measure for Ergodic Markov process. (20)**
- Q.7 What is traffic engineering? Explain the terms busy hours, traffic intensity and grade of service. What are the delay systems in telecommunication network? (20)**

UNIT-IV

- Q.8 Explain different services supported by ISDN with suitable diagrams. (20)**
- Q.9 Explain ISDN network architecture in detail. (20)**

*****ETE MAY/JUNE 2018*****